IOSR Journal of Electrical and Electronics Engineering (IOSR-JEEE)
e-ISSN: 2278-1676,p-ISSN: 2320-3331
PP 58-64
www.iosrjournals.org

Design and Analysis of Semi-Transparent Flip-Flops for high speed and Low Power Applications in Networks

Mr.Kaustubh Kumar Shukla[1], Ms.G.Komala Yadav[2]
[1]Department of ECE, Sree Vidyanikethan Engineering College, Tirupati, A.P.,India
[2]Department of ECE, Sree Vidyanikethan Engineering College, Tirupati, A.P.,India

Abstract: *In the research of low power and low voltage in networks, the use and implementation of dual edge triggered flip flop has gained more attention at the gate level design. The main advantage of using dual edge triggered flip flop is that it allows one to maintain a constant throughput while operating at only half the clock frequency. This paper proposes a dual edge triggered flip flop (DETFF) for optimization of energy, power and delay. Results are compared with four previously published static edge triggered flip-flops for their performance, power dissipation, low voltage and low power applications. For each DETFF the optimal delay, power consumption and energy are determined as the primary figure of merit. The proposed design demonstrates the least energy at low voltages. A dual-edge sense amplifier flip-flop (DE-SAFF) for resonant clock distribution networks (CDNs) is proposed. The clocking scheme used to enable dual-edge triggering in the proposed SAFF reduces short circuit power by allowing the pre-charging transistors to be switched on only for a portion of the clock period. The extracted circuit layout of the proposed DE-SAFF has been simulated with a resonant clock signal at a frequency of 500 MHz. Simulation results show correct functionality of the flip-flop under process, voltage and temperature variations. Two low-power clocking techniques, the dual-edge triggering method and the emerging resonant (sinusoidal) clocking technique, have been combined to enable further power reduction in the CDN. Modeling the resonant clock distribution system with the proposed flip-flop illustrates that dual-edge triggering can achieve up to 58% reduction in the power consumption of resonant clock networks.*

***Index Terms*:** *Clock-gated, high-performance, low-power, sense-amplifier flip-flop.*

I. Introduction

In pulsed dual-edge triggered sense-amplifier flip-flop (DET-SAFF) for low-power and high-performance applications is presented in this paper. By incorporating the dual-edge triggering mechanism in the new fast latch and employing conditional pre charging, the DET-SAFF is able to achieve low-power consumption that has small delay. To further reduce the power consumption at low switching activities, a clock-gated sense-amplifier (CG-SAFF) is engaged. Extensive post-layout simulations proved that the proposed DET-SAFF exhibits both the low-power and high-speed properties, with delay and power reduction of up to 43.3% and 33.5% of those of the prior art, respectively. When the switching activity is less than 0.5, the proposed CG-SAFF demonstrates its superiority in terms of power reduction. During zero input switching activity, CG-SAFF can realize up to 86% in power saving. Lastly, a modification to the proposed circuit has led to an improved common-mode rejection ratio (CMRR) DET-SAFF.

II. Review of DET-SAFF For Low Power

Power consumption and timing delays are the two important design parameters in high speed VLSI systems. In many digital very large scale integration (VLSI) designs, the clock system that includes clock distribution network and flip-flops, is one of the most power consumption components. It accounts for 30% to 60% of the total system power where 90% of which is consumed by the flip-flops and the last branches of the clock distribution network that is driving the flip-flop. As clock frequency increases the latency of the flip-flop or latch will play an even greater role in the overall cycle time.

A Flip-Flop that synchronizes the state changes during a clock pulse transition is the edge-triggered flip-flop. When the clock pulse input exceeds a specific threshold level, the inputs are locked out and the flip-flop is not affected by further changes in the inputs until the clock pulse returns to 0 and another pulse occurs. As the clock frequency increase, pulse-triggered flip-flop tends to be popular as compared to conventional master-slave flip-flops. Because they employ time borrowing across cycle boundaries which results in zero or negative setup time. Moreover, the number of transistors we used in the pulse-triggered flip-flop is less than the number we used in the conventional master-slave flip-flops.

To evaluate the performance of the proposed flip-flops, comparisons had been performed with other dual edge-triggered designs, including SCDFF DSPFF and ACSAFF. All the flip-flops were designed using Chartered Semiconductor Limited's 0.18- m CMOS process technology, at an operating temperature of 27 and a supply voltage of 1.8 V, using Cadence SPECTRE. The designs were optimized for a clock frequency of 0.8 GHz. A load capacitance of 100 pF was used for all outputs. All the measurements were taken over a 16-cycle data sequence of alternating 1's and 0's. The performances of all the flip-flops were measured based on their post-layouts results with all parasitic extracted and back annotated in the circuit simulation environment. The proposed DET-SAFF has the minimum power consumption when the switching activity is greater than 0.5. At maximum input switching activity, DET-SAFF offers 20.3%, 23.2%, 33.5%, and 26% power reductions as compared to SCDFF [8], DSPFF [9], ACSAFF [10], and the proposed CG-SAFF. ACSAFF and CG-SAFF consume more power at high input switching activities due to the addition of the control circuits in the pulse generating paths. However, CGSAFF exhibits its superiority in power saving when the input switching activity is less than 0.5. With an input switching activity of 0.25, the power consumption of CG-SAFF is 20.8%,27.6%, 7%, and 7.6% less than SCDFF, DSPFF, ACSAFF, and the proposed DET-SAFF, respectively. The highest reduction of power consumption is achieved when D is idle. And in this case, the power saving is more than 75% as compared to all other reported flip-flops.

III. Proposed dual-edge triggered flip-flops

A. Static Output-Controlled Discharge Flip-Flop

SCDFF involves an explicit pulse generator and a latch that captures the pulse signal. The latch structure of SCDFF consists of two static stages. In the first stage, input D is used to drive the pre charge transistor so that node X follows D during the sampling period. In addition, the conditional discharging technique is implemented by inserting a QB-controlled nMOS in the discharge path, which prevents unnecessary discharging at node X as long as the input remains high. The major advantage of SCDFF is low power consumption and soft-edge property. However, a delay is always presented between Q and QB due to the single-ended nature of SCDFF.

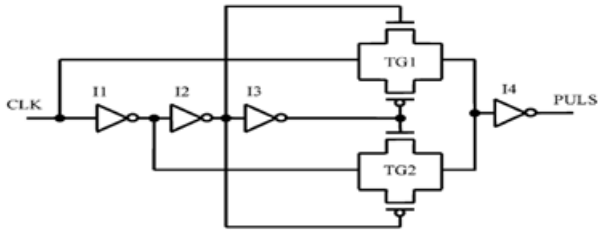

FIG.1 Static Output-Controlled Discharge Flip-Flop

B.Adaptive Clocking Dual Edge-Triggered Sense-Amplifier Flip-Flop

ACSAFF is an implicit dual-edge triggered sense amplifier flip flop. It consists of three stages, i.e., the adaptive clock inverting stage, the front-end sensing stage and the Nikolic's latch [11] stage. The adaptive clock inverter chain is designed to disable some internal clocked transistors when the data switching activity is low. The signal derived from node NC of the sensing stage is used to implement adaptive clocking. If input D is different from output Q, node NC will be pulled up, to turn on transistors N1 and N2. Consequently, the desired inverted and delayed signals, CLK3 and CLK4, will be produced so that a narrow transparent window is created on the rising or falling edges of the clock. Once the output state is altered, the charging path of NC is blocked and NC will be discharged through either N3 and N4 or N5 and N6, thereby disabling the inverter chain. When D is the same as Q, node NC is low and the flip-flop is opaque. ACSAFF obtains great power reduction at low switching activity. Nevertheless, the adaptive clocking requires more transistors and hence causing the circuit to be more complex. This will lead to greater power consumption at high switching activity and the degradation of the flip-flop speed.

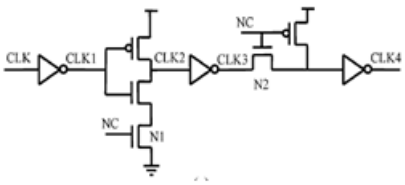

FIG.2 Adaptive Clocking Dual Edge-Triggered Sense-Amplifier Flip-Flop

C.Dual-Edge Triggered Flip-Flops

It consists of three stages: the pulse generating stage, the sensing stage and the latching stage. The simple pulse generator used in DETSAFF is the same as that of [13]. The dual edge triggered pulse generator produces a brief pulse signal synchronized at the rising and falling clock edges. The pulse generator can be shared by multiple flip-flop circuits when a group of flip-flops are located closely.

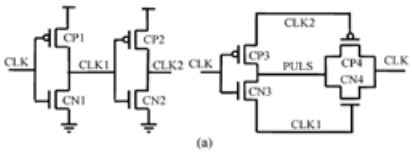

FIG.3 Dual Pulse Generator

For a sense amplifier based flip-flop, in the evaluation phase, as soon as D is low, SB will be set to high, and if D is high, RB will be set to high. Therefore, the conditional pre charging technique is applied in the sensing stage of DET-SAFF, to avoid redundant transitions at major internal nodes. Two input controlled pMOS transistors, SP1 and SP2, are embedded in the pre charge paths of nodes SB and RB, respectively. In this case, if D remains high for n cycles, SB may only be discharged in the first cycle. For the following cycles, SB will be floating when PULS is low or fed to the low state DB when PULS is high. As for RB, it only needs to be pre charged in the first cycle and remains at its high state for the remaining cycles. Since the pre charging activity is conditionally controlled, the critical pull down path of SB and RB is simplified, consisting of only one signal transistor. This helps to reduce the discharging time significantly. As such, the resulting sensing stage possesses low-power and high-speed features.

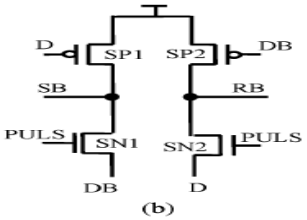

FIG.4 Sensing Stage

To further improve the operating speed, a fast symmetric latch is developed. Similar to the Nikolic's latch and Strollo's latch [14], the new latch makes use of SB and RB to pull up the output nodes. But the pull down path is modified. It composes a PULS-controlled nMOS pass transistor, through which D (DB) is directly fed to the Q (QB) node. On the other hand, the low-to-high latency will also be improved. This is because the output node will not only be charged by the pull-up transistors, LP1 and LP2, but also the pass transistors, LN1 and LN2. Note that the pass transistors cannot fully charge a node to high, but it can assist with the pull-up transition. The four inner transistors, LP3, LP4, LN3, and LN4, are of minimum sizes, serving the purpose of maintaining the output state when the flip-flop is opaque.

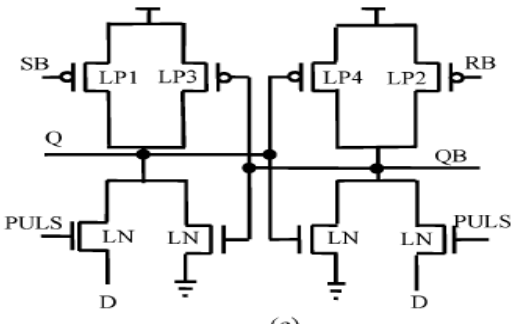

FIG.5 Symmetric Diagram

For the proposed DETSAFF and previously mentioned dual edge designs, such as the SCDFF and DSPFF, the power saving techniques are only applicable for the latch part of the flip-flops. As the switching activity of the clock signal is 1, the pulse generator will always be operating even when the input invokes no output changes. These unnecessary transitions cause a lot of power to be wasted, especially at low input

switching activities. Dual-Edge Triggered Clocked Storage Elements (DETSE) –storage elements capable of capturing data on both clock edges. Goal to reduce power consumption of the clock distribution tree by reducing the clock frequency.

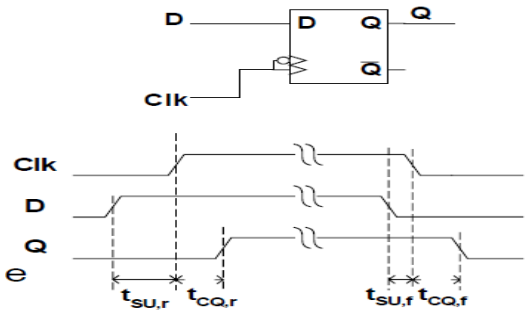

FIG.6 D-Flip Flop

IV. Simulation Methodology And performance Comparisons

To evaluate the performance of the proposed flip-flops, comparisons had been performed with other dual edge-triggered designs, including SCDFF [8], DSPFF [9], and ACSAFF [10]. All the flip-flops were designed using Chartered Semiconductor Limited's 0.18- m CMOS process technology, at an operating temperature of 27 and a supply voltage of 1.8 V, using Cadence SPECTRE. The designs were optimized for a clock frequency of 0.8 GHz. A load capacitance of 100 fF was used for all outputs. All the measurements were taken over a 16-cycle data sequence of alternating 1's and 0's. The performances of all the flip-flops were measured based on their post-layouts results with all parasitic extracted and back annotated in the circuit simulation environment.

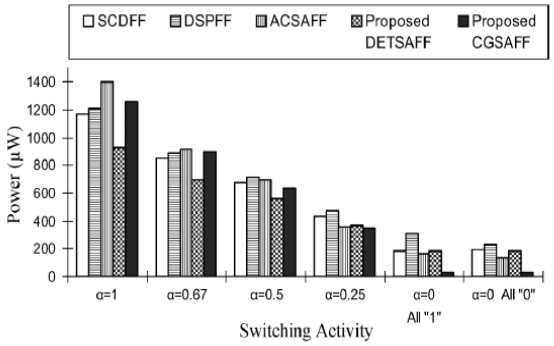

FIG.6 Comparison of Existed & Proposed system

The proposed DET-SAFF has the minimum power consumption when the switching activity is greater than 0.5. At maximum input switching activity, DET-SAFF offers 20.3%, 23.2%, 33.5%, and 26% power reductions as compared to SCDFF [8], DSPFF [9], ACSAFF [10], and the proposed CG-SAFF. ACSAFF and CG-SAFF consume more power at high input switching activities due to the addition of the control circuits in the pulse generating paths. However, CGSAFF exhibits its superiority in power saving when the input switching activity is less than 0.5.With an input switching activity of 0.25, the power consumption of CG-SAFF is 20.8%, 27.6%, 7%, and 7.6% less than SCDFF, DSPFF, ACSAFF, and the proposed DET-SAFF, respectively. The highest reduction of power consumption is achieved when D is idle. And in this case, the power saving is more than 75% as compared to all other reported flip-flops.

Designs	SCDFF [8]	DSPFF [9]	ACSAFF [10]	DET-SAFF	CG-SAFF
CLK-to-Q delay (ps)	172.4	206.9	176.4	117.2	152.4
Min D-to-Q delay (ps)	169.4	157.8	421.1	93.42	307
Setup time (ps)	-98	-128	180	-70	90
Hold time (ps)	357	252	222	258	199
MOCF* (GHz)	1	1.43	0.83	1	1.25
# of transistors	29	24	39	22	40
Total width (μm)	55.64	66.82	114.46	55.59	96.52
Layout Area $(\mu m)^2$	199.5	189.9	261.7	157.85	267.6

Table-1 Comparison table

In an attempt to improve the CMRR of the proposed DETSAFF, which has been analyzed to be 1 we modified the sensing stage of the proposed DET-SAFF. An additional pMOS transistor SP3 is added to the proposed design and the circuit is renamed mDET-SAFF. In mDET-SAFF, transistors SN1 and SN2 are controlled by D and DB, respectively. The additional transistor SP3 is triggered by the\ clock pulse signal PLUS, thus reducing the load on the clock pulse from two transistors to one transistor and with improved CMRR.

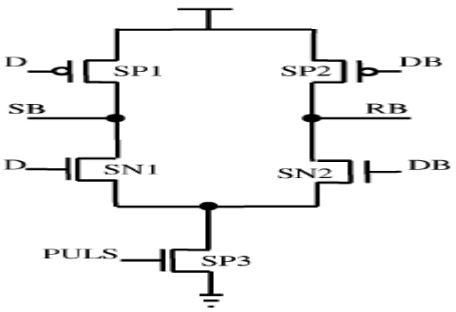

FIG.7 Modified sensing stage of DET-SAFF

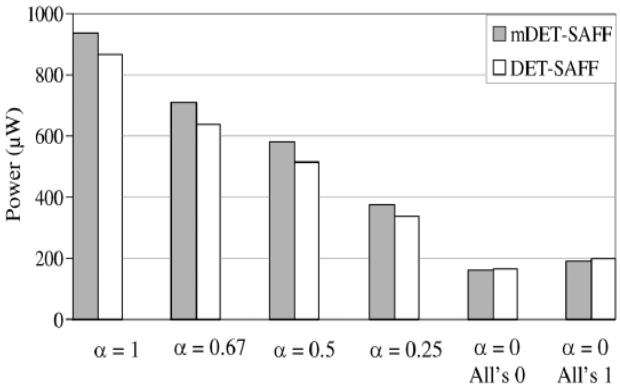

Table-2 Compare of DET-SAFF & mDET-SATFF

The comparison results on power dissipation at different input switching activities between the proposed DET-SAFF and mDET-SAFF with respect to PDP, the mDET-SAFF consumes 6.5% more PDP as compared to the proposed DET-SAFF. However, the modified version of the proposed DET-SAFF has a much improved CMRR than that of the proposed DET-SAFF.

V. Result And Implementation

The output of dual edge trigger sense amplifier flip flop successfully obtained using Model SIM. Therefore switching activity, speed and power reduced.

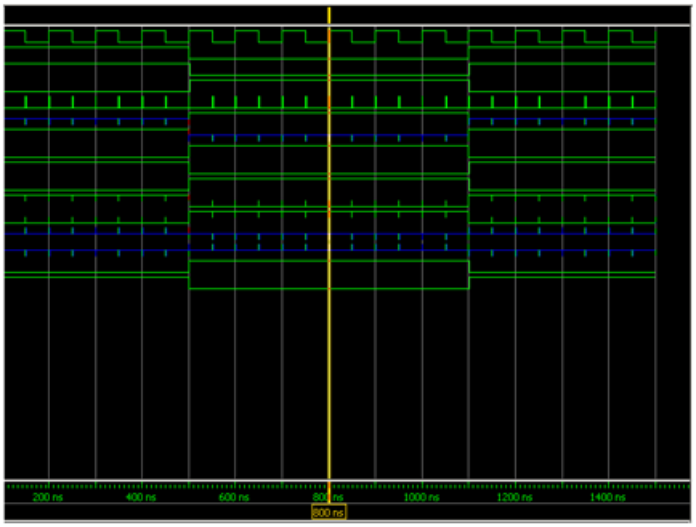

Fig.8 Output of symmetric latch

VI. Conclusion

This paper presents two novel dual-edge triggered flip-flops for low power and high performance applications. DET-SAFF achieves substantial power reduction by incorporating dual-edge triggering and conditional pre charging. It also minimizes latency by utilizing a fast latch. In addition, it has a negative setup time of 70 ps which provide useful attribute to time borrowing and clock uncertainty absorption. CGSAFF is superior in power saving at low switching activities. As compared to ACSAFF, which also has a power saving pulse generator, CG-SAFF outperforms in terms of power consumption (maximum of 75%), latency (27%), setup time (50%) and operation stability. Furthermore, a modified version of the DET-SAFF is introduced, which significantly improves the CMRR. Although this modified version consumes about 5% more power than the proposed DET-SAFF, both versions of the proposed DET-SAFFs have conclusively proved their robustness and suitability of applications when low power and high speed are of equal importance.

References

[1]. H. Kawaguchi and T. Sakurai, "A reduced clock-swing flip-flop(RCSFF) for 63% power reduction," *IEEE J. Solid State Circuits*, vol.33, no. 5, pp. 807–811, May 1998.

[2]. N. Nedovic, M. Aleksic, and V. G. Oklobdzija, "Conditional precharge techniques for power-efficient dual-edge clocking," in *Proc. 2002 Int. Symp. Low Power Electronics Design (ISPLED 2002)*, 2002, pp.56–59.

[3]. C.-C. Yu, "Design of low-power double edge-triggered flip-flop circuit," in *Proc. 2nd IEEE Conf. Industrial Electronics Applications.(ICIEA 2007)*, May 2007, pp. 2054-2057.

[4]. C. S. Kim, J. S. Kong, Y. S. Moon, and Y. H. Jun, "Presetting pulsebased flip-flop," in *Proc. IEEE Int. Symp. Circuits Systems (ISCAS 2008)*, May 2008, pp. 588–591.

[5]. P. Zhao *et al.*, "Low-power clock branch sharing double edge-triggered flip-flop," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 15, no. 3, pp. 338–345, Mar. 2007.

[6]. P. Zhao, T. K. Darwish, and M. A. Bayoumi, "High-performance and low-power conditional discharge flip-flop," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 12, no. 5, pp. 477–484, May 2004.

[7]. B. S. Kong, S. S. Kim, and Y. H. Jun, "Conditional-capture flip-flop for statistical power reduction," *IEEE J. Solid-State Circuits*, vol. 36, no. 8, pp. 1263–1271, Aug. 2001.

[8]. M. W. Phyu, W. L. Goh, and K. S. Yeo, "A low-power static dual edgetriggered flip-flop using an output-controlled discharge configuration,"in *Proc. IEEE Int. Symp. Circuits Systems (ISCAS 2005)*, May 2005,vol. 3, pp. 2429–2432.

[9]. G. Aliakbar and M. Hamid, "Dual-edge triggered static pulsed flip-flops," in *Proc. 18th Int. Conf. VLSI Design 2005*, Jan. 2005, pp.846–849.

[10]. Y. T. Liu, L. Y. Chiou, and S. J. Chang, "Energy-efficient adaptive clocking dual edge sense-amplifier flip-flop," in *Proc. IEEE Int. Symp.Circuits Systems (ISCAS 2006)*, May 2006, pp. 4329–4332.

[11]. B. Nikolic, V. G. Oklobdzija, V. Stajanovic, W. Jia, J. K. Chiu, and M.M. Leung, "Improved sense-amplifier based flip-flop: Design and measurements,"*IEEE J. Solid-State Circuits*, vol. 35, no. 6, pp. 876–883,Jun. 2000.

[12]. P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuit*. New York: Wiley, 2000.

[13]. J. I. Kim and B. S. Kong, "Dual edge-triggered flip-flop with modified NAND keeper for high-performance VLSI," *Current Appl. Phys.*, vol.4, no. 1, pp. 49–53, Feb. 2004.
[14]. A. G. M. Strollo, D. De Caro, E. Napoli, and N. Petra, "A novel highspeed sense-amplifier-based flip-flop," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 13, no. 11, pp. 1266–1274, Nov. 2005.
[15]. C. K. The, M. Hamada, T. Fujita, H. Hara, N. Ikumi, and Y. Oowaki,"Conditional data mapping flip-flops for low-power and high-performance systems," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*,vol. 14, no. 12, pp. 1379–1383, Dec. 2006.
[16]. M. Sharma, Dr A. Noor, S. Tiwari, K. Singh (2009), "An Area and Power Efficient design of Single Edge Triggered D-Flip Flop", in Proc. IEEE International Conference on Advances in Recent Technologies in Communication and Computing,2009, pp. 478-481.
[17]. M. Sharma, K. G. Sharma,T. Sharma,Prof.B. P. Singh, N. Arora (2011), "Modified SET D Flip Flop for Low Power VLSI Application",IEEE (2011), pp. 1-5.
[18]. Jin-Fa Lin, **"**Low-Power Pulse-Triggered Flip-Flop Design Based on a Signal Feed-Through Scheme" *IEEE Trans, Very Large Scale Integr. (VLSI) Syst.,* 1063 8210/$31.00 © 2013 *IEEE*